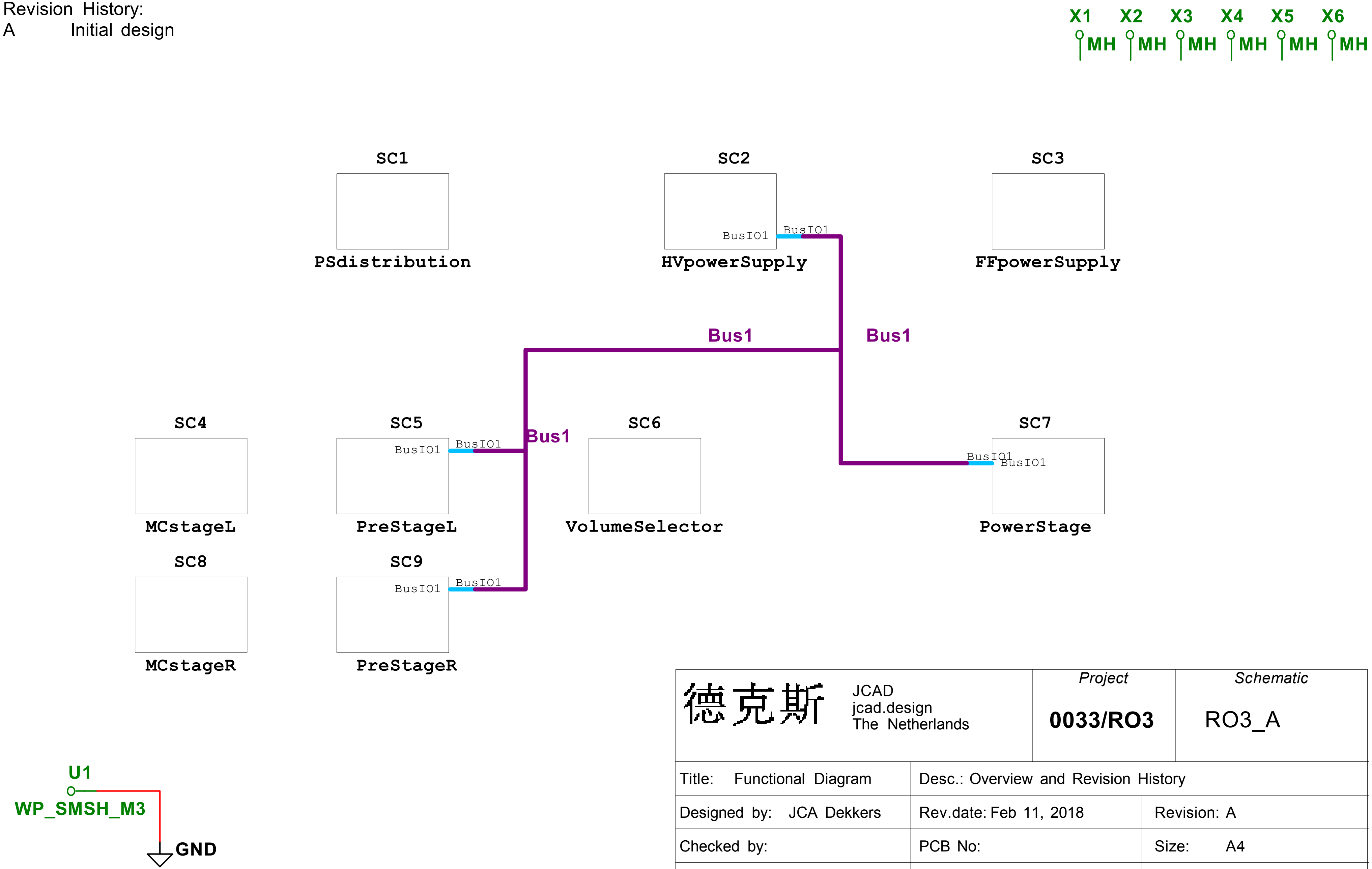
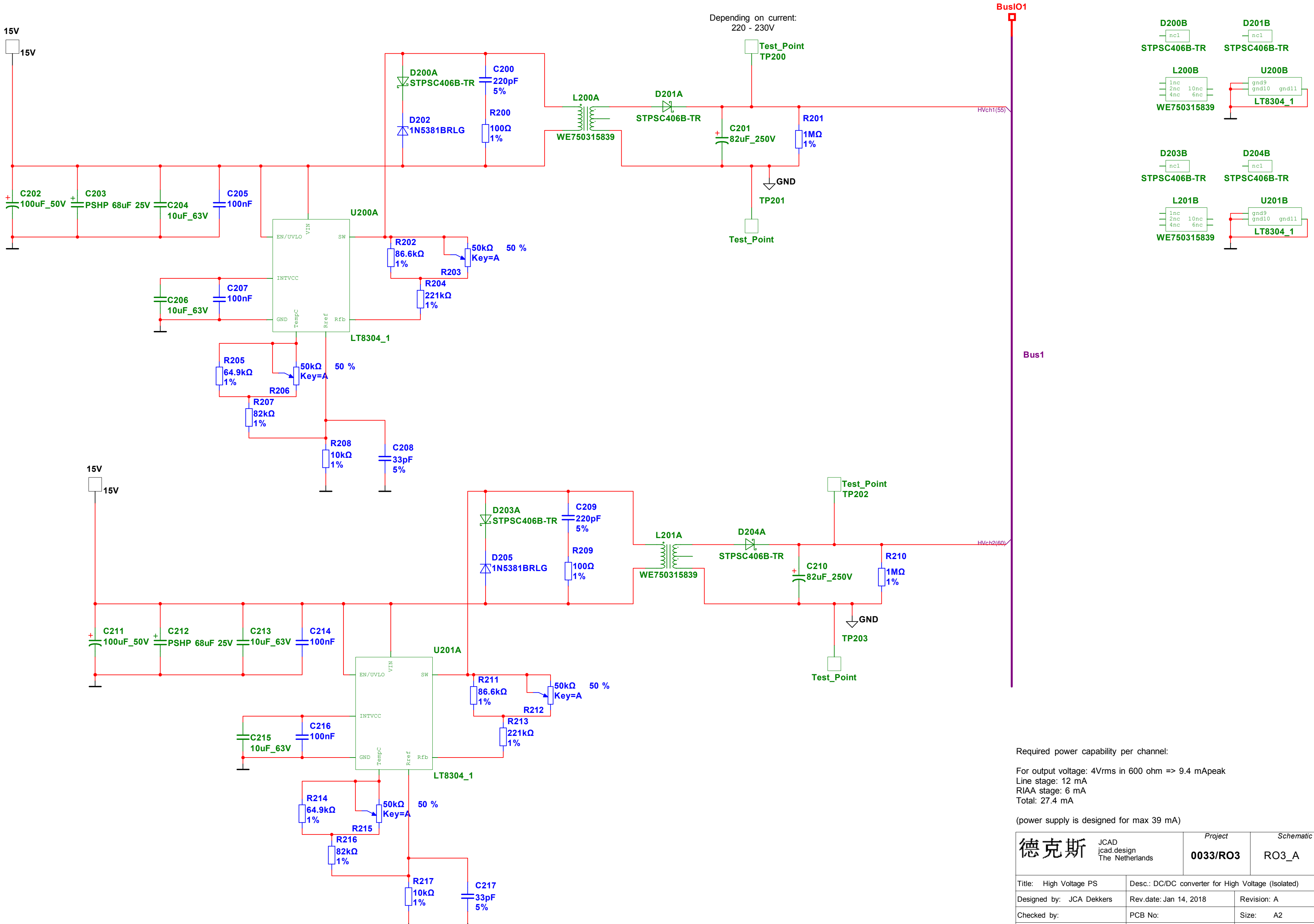
Revision History:
A Initial design



德克斯 JCAD jcad.design The Netherlands		*Project* 0033/RO3	*Schematic* RO3_A
Title: Functional Diagram	Desc.: Overview and Revision History		
Designed by: JCA Dekkers	Rev.date: Feb 11, 2018	Revision: A	
Checked by:	PCB No:	Size: A4	
Approved by:	Sheet 1 of 10	1st.date: Nov 4, 2017	



Required power capability per channel:

For output voltage: 4Vrms in 600 ohm => 9.4 mApeak
Line stage: 12 mA
RIAA stage: 6 mA
Total: 27.4 mA

(power supply is designed for max 39 mA)

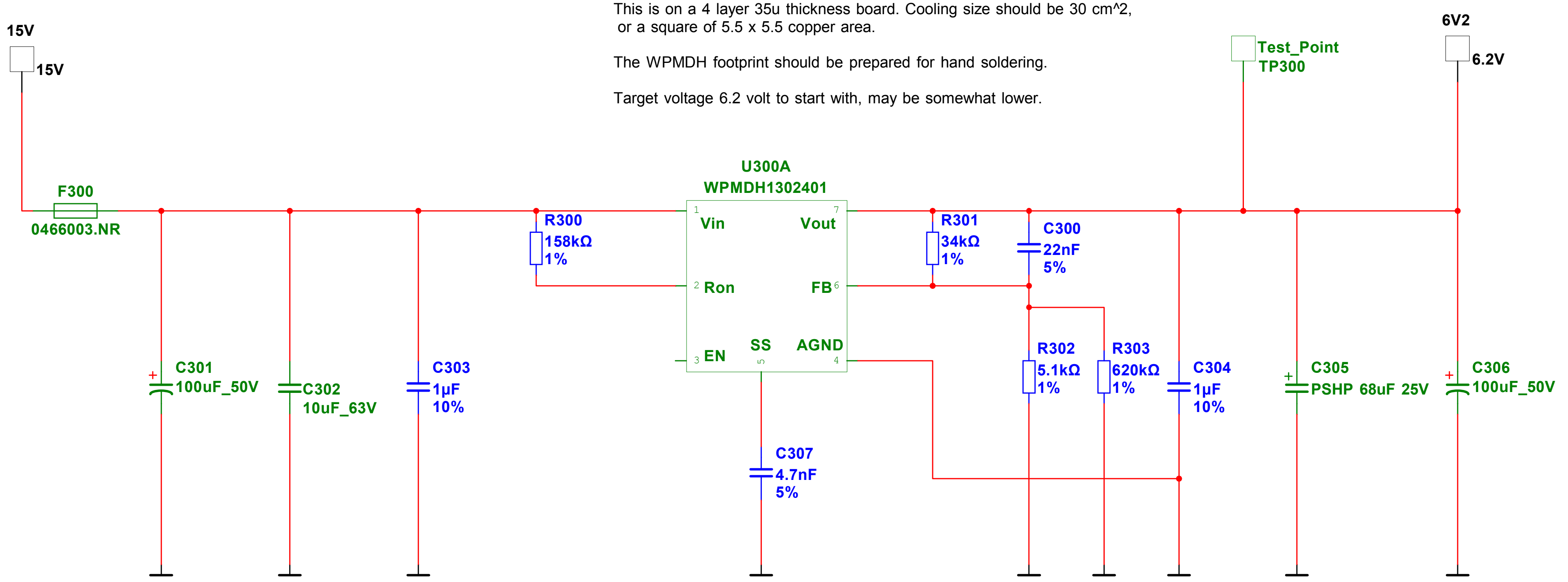
Attenuator calculator: http://amorgignitamorem.nl/WebPaginas/Attenuator/AttenuatorAccordingToRonEnJacco.html

德克斯 JCAD jcad.design The Netherlands	Project: 0033/RO3	Schematic: RO3_A
Title: High Voltage PS	Desc.: DC/DC converter for High Voltage (Isolated)	
Designed by: JCA Dekkers	Rev.date: Jan 14, 2018	Revision: A
Checked by:	PCB No:	Size: A2
Approved by:	Sheet 2 of 10	1st.date: Dec 26, 2017

For 2.5 A ampere one needs 22 K/W thermal resisantce (see datasheet).
This is on a 4 layer 35u thickness board. Cooling size should be 30 cm^2,
or a square of 5.5 x 5.5 copper area.

The WPMDH footprint should be prepared for hand soldering.

Target voltage 6.2 volt to start with, may be somewhat lower.



AGND should be connected
to 1uF Cout as short as possible.

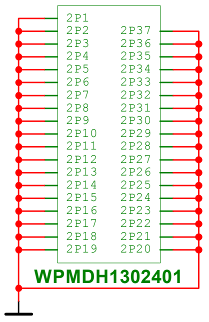
Design procedure:
1a. Rfbt/Rfbb = (Vout/0.803) - 1 = 6.72...
1b. Resistors should be between 1k ... 50k
1c. Choose Rfbt = 34k => Rfbb = 5.059 k

2a. Fsw(ccm) should be between 200kHz...800kHz, target 300kHz
2b. Ron = Vout/(1.3e-10 * Fsw(ccm)) => 158k
2c. Check whether Ron equal or greater than Vinmax*150e-9/1.3e-10 => okay!

With Vin = 15, Vout = 6.2 and Fsw = 300k the DCM/CCM boundary is at approx 600 mA.

3a. Worst case input ripple current 0.5*Iout*sqrt(D/(1-D)) => 1.18 A. Input C should be able to withstand this.
3b. Value of Cin is related to the maximum DeltaVin: Cin equal or greater than Iout*D*(1-D)/(Fsw(ccm)*DeltaVin) => 100uF safe choice

U300B

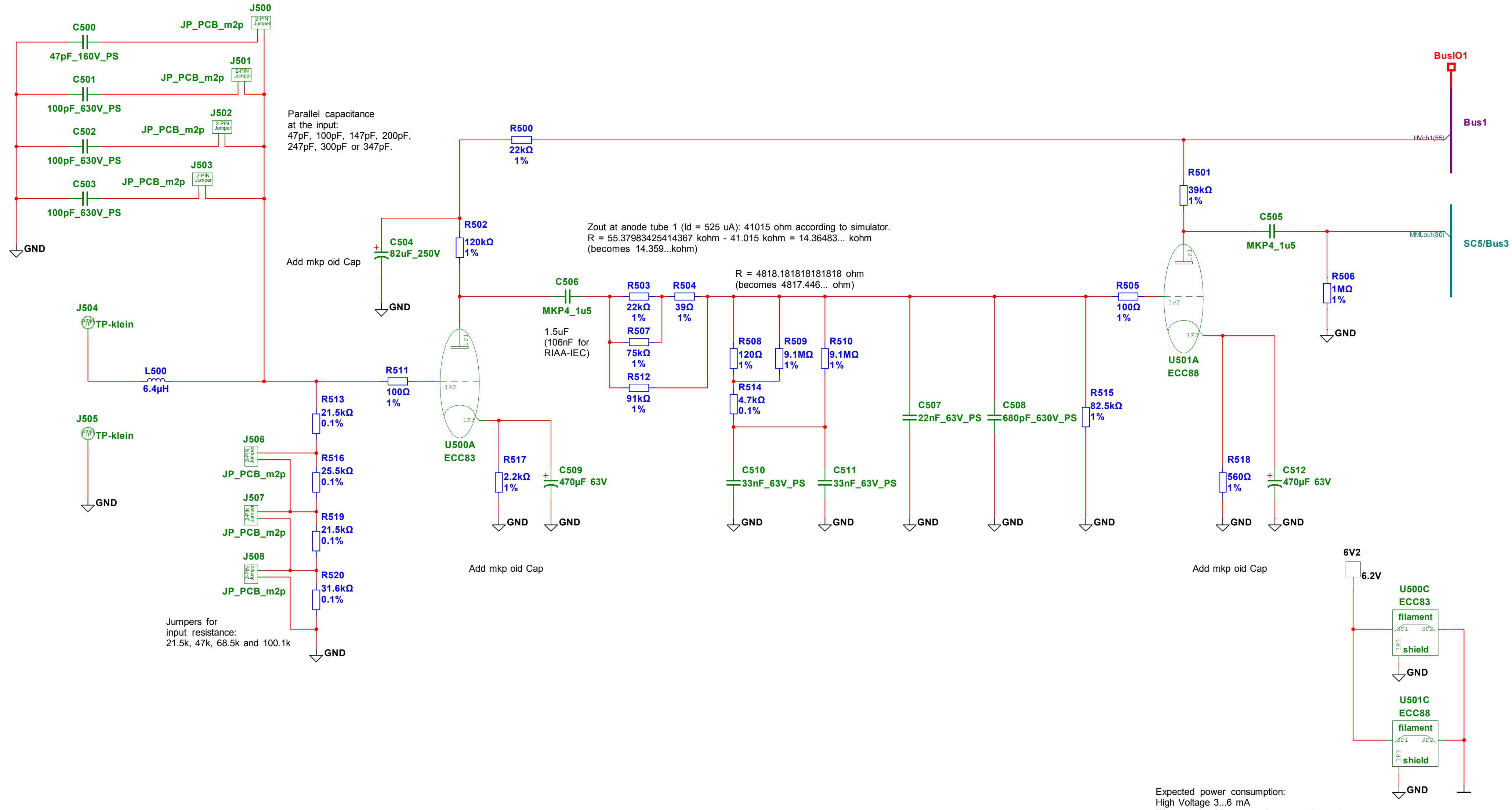


WPMDH1302401

Required power capability:
Filament: 6.3V at 2 x 1.095...1425 mA = 2.19...2.85 A

德克斯 JCAD jcad.design The Netherlands		*Project* 0033/RO3	*Schematic* RO3_A
Title: Filament PS	Desc.: DC/DC power supply for filaments		
Designed by: JCA Dekkers	Rev.date: Jan 14, 2018	Revision: A	
Checked by:	PCB No:	Size: A3	
Approved by:	Sheet 3 of 10	1st.date: Dec 24, 2017	

Total Gain = 40 dB

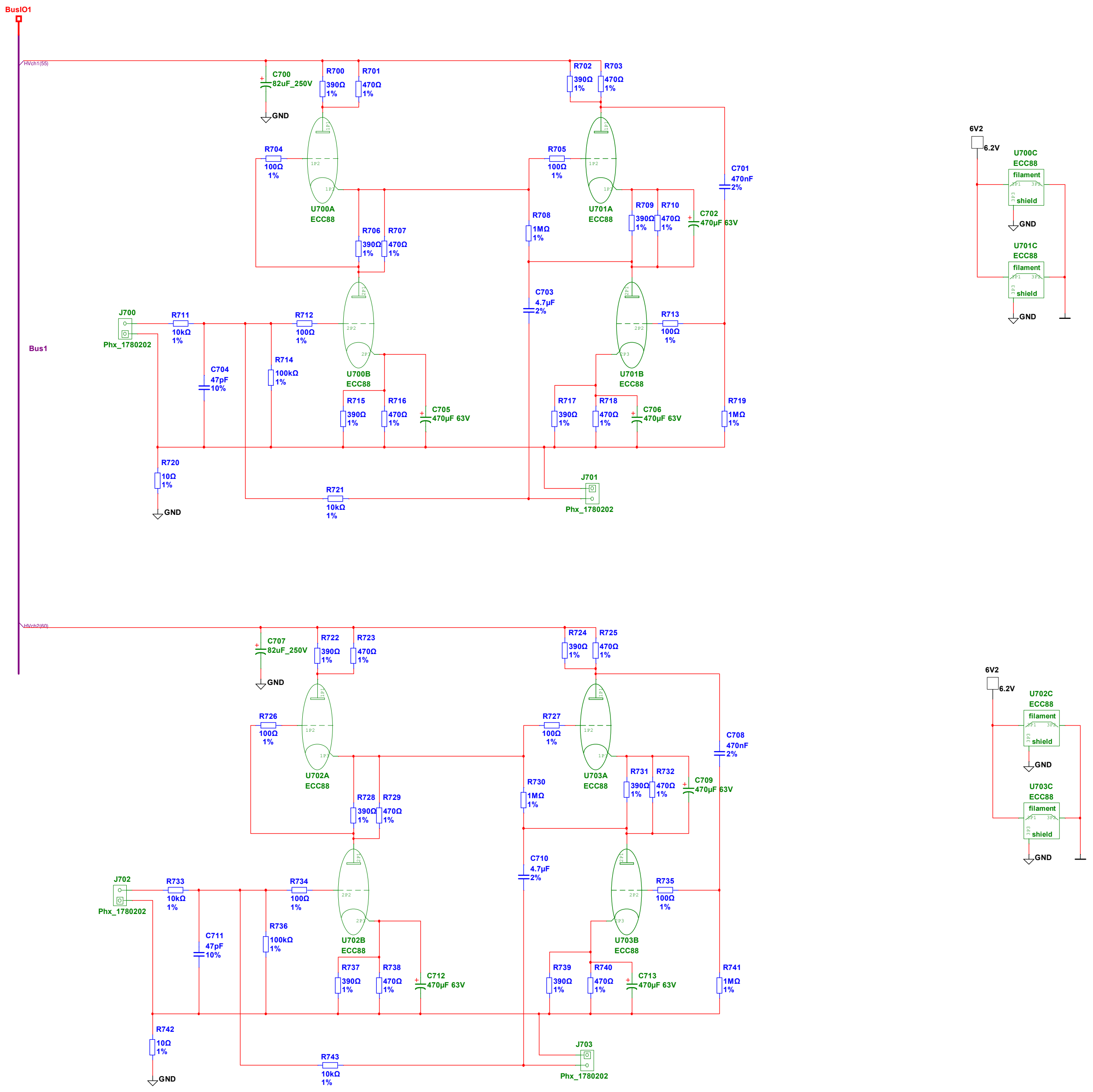


Capacitors: LCR Components FSC(/EX) series
Resistors: TE Connectivity/Neohm H8 (Holco), R series
Welwyn RC, RC55, PR (low cost) series
Vishay Dale PTF series
http://nl.farnell.com/webapp/wcs/stores/servlet/Search?catalogId=15001&langId=31&storeId=10168&categoryId=700000005447&pageSize=25&showResults=true&sf=432,502,721&pf=110003727,110075262,110101775,110124724,112067013

Passive RIAA calculator: http://amorgignitamorem.nl/WebPaginas/passieve_RIAA/passieve_RIAA.html

德克斯 JCAD jcad.design The Netherlands	Project 0033/RO3	Schematic RO3_A
Title: MM RIAA stage (left)	Desc.: Passive RIAA and Input Impedance Selection	
Designed by: JCA Dekkers	Rev.date: Feb 04, 2018	Revision: A
Checked by:	PCB No:	Size: A2
Approved by:	Sheet 4 of 10	1st.date: Nov 4, 2017

德克斯 JCAD jcad.design The Netherlands		*Project* **0033/RO3**	*Schematic* RO3_A
Title: Input Selection	Desc.: RO3_A		
Designed by: JCA Dekkers	Rev.date: Jan 14, 2018	Revision: A	
Checked by:	PCB No:	Size: A3	
Approved by:	Sheet 5 of 10	1st.date: Nov 4, 2017	



Bandwidth 7 MHz

f = 1 kHz, B = 20 Hz - 30 kHz:

Vin,rms	Vout,rms	THD+N [%]	SNR [dB]
0.0707	0.0645	0.008	82.0
0.707	0.645	0.0023	98.6
2.0	1.82	0.0021	105.1
4.0	3.64	0.0038	101.2

With 50 ohm source and 2.2 kohm load (optimum load).

Vin,dc = 0 mV
Vout,dc = 0 mV

f = 1kHz at -0.92 dB, 20 Hz at -0.96 dB, 20 kHz at -0.92 dB, 100 kHz at -0.94 dB
Without feedback (R23 desoldered): Av = 25.56 dB at 1 kHz.

Rin = 10k4 (1 kHz), Rout = 36 ohm (20 Hz), 12 ohm (1 kHz and 10 kHz).

4u7:
Audyn Cap Plus, 1341762
D = 36mm, L = 63mm, d2 = 1.5mm

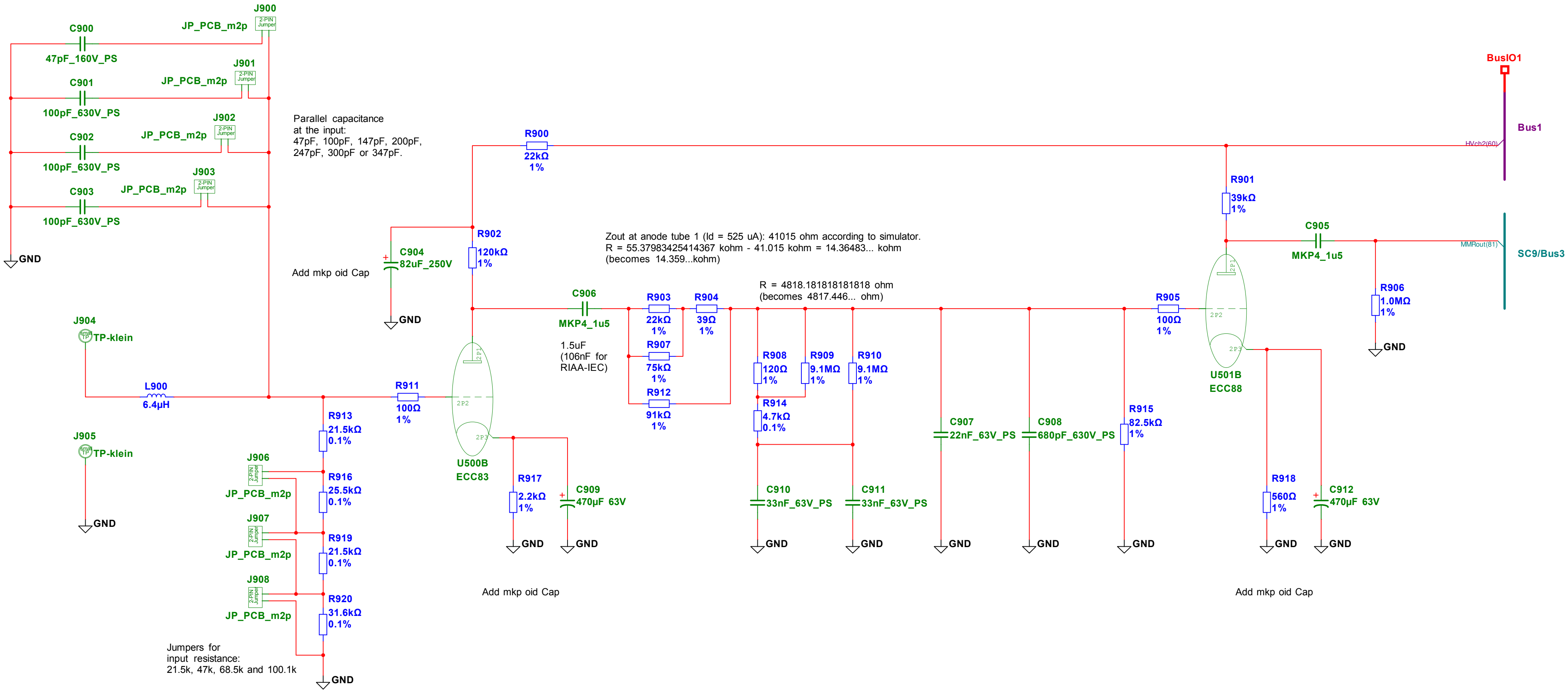
Audyn Cap Plus, 1341758
D = 25mm, L = 43mm, d2 = 1mm

Audyn Cap Plus, 1341755
D = 25mm, L = 43mm, d2 = 1mm

Expected power consumption:
High Voltage 12 mA
Filament: 2 x 365...475 mA = 950 mA worst case

德克斯 JCAD jcad.design The Netherlands		Project: 0033/RO3	Schematic: RO3_A
Title: Line Driver	Desc.: 2 Channel SRPP/White with feedback		
Designed by: JCA Dekkers	Rev.date: Jan 14, 2018		Revision: A
Checked by:	PCB No:		Size: A1
Approved by:	Sheet 6 of 10		1st.date: Nov 4, 2017

Total Gain = 40 dB

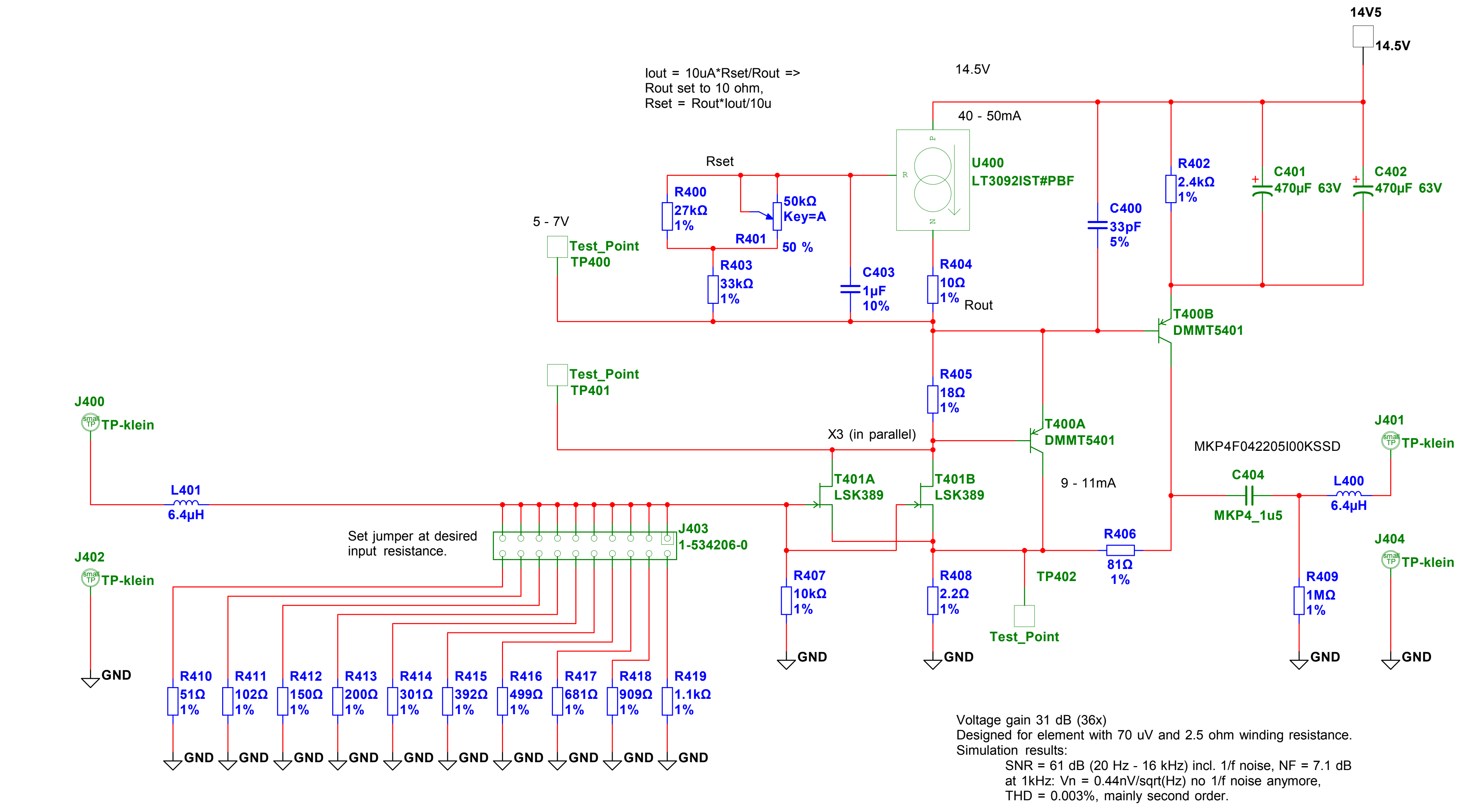


Expected power consumption:
High Voltage 3...6 mA
Filament: 1 x 365...475 mA = 475 mA worst case

德克斯 JCAD jcad.design The Netherlands		Project 0033/RO3	Schematic RO3_A
Title: MM RIAA stage (right)	Desc.: Passive RIAA and Input Impedance Selection		
Designed by: JCA Dekkers	Rev.date: Feb 04, 2018	Revision: A	
Checked by:	PCB No:	Size: A2	
Approved by:	Sheet 7 of 10	1st.date: Nov 4, 2017	

Capacitors: LCR Components FSC(/EX) series
Resistors: TE Connectivity/Neohm H8 (Holco), R series
Welwyn RC, RC55, PR (low cost) series
Vishay Dale PTF series
http://nl.farnell.com/webapp/wcs/stores/servlet/Search?catalogId=15001&langId=31&storeId=10168&categoryId=700000005447&pageSize=25&showResults=true&sf=432,502,721&pf=110003727,110075262,110101775,110124724,112067013

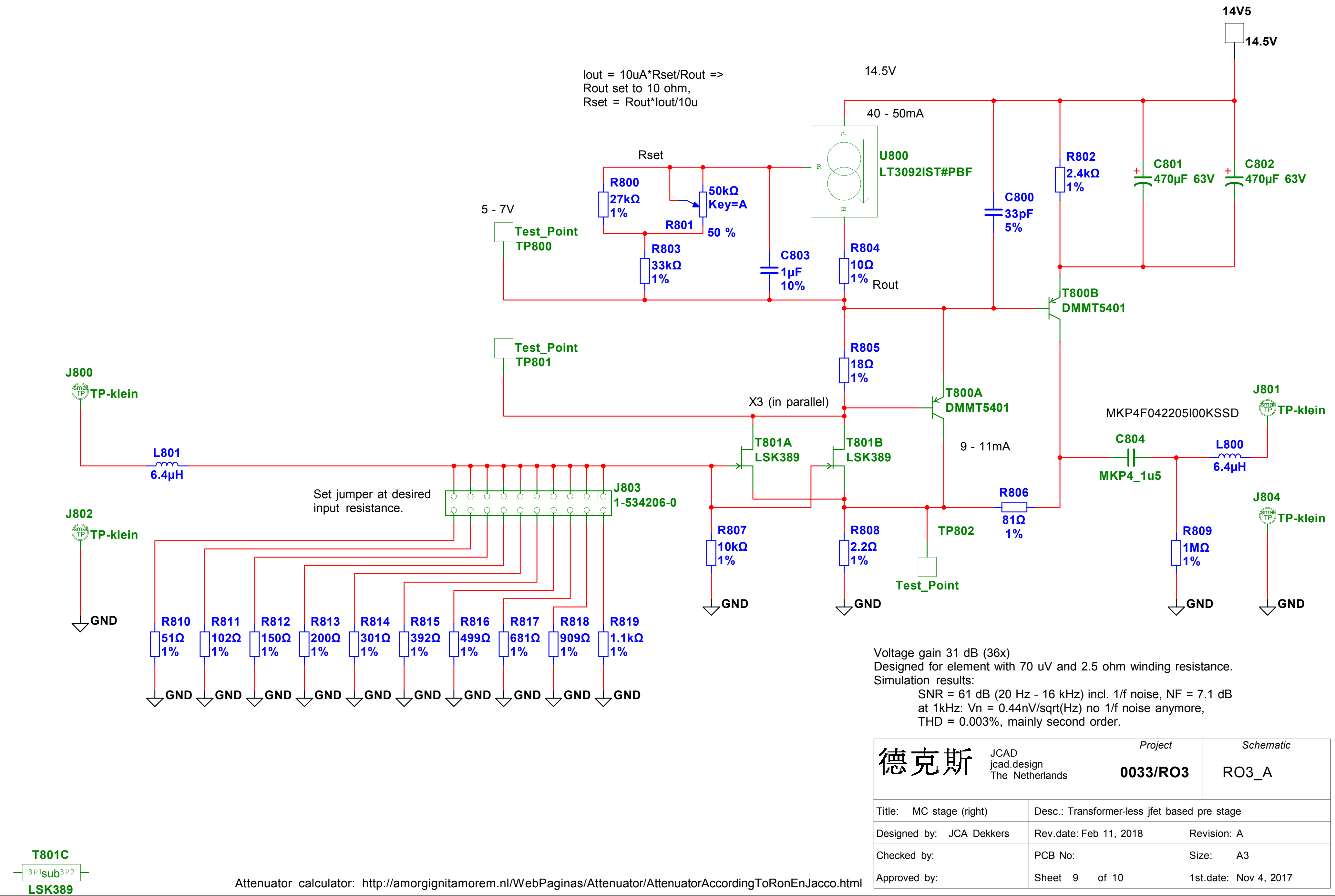
Passive RIAA calculator: http://amorgignitamorem.nl/WebPaginas/passieve_RIAA/passieve_RIAA.html



Voltage gain 31 dB (36x)
Designed for element with 70 uV and 2.5 ohm winding resistance.
Simulation results:
SNR = 61 dB (20 Hz - 16 kHz) incl. 1/f noise, NF = 7.1 dB
at 1kHz: Vn = 0.44nV/sqrt(Hz) no 1/f noise anymore,
THD = 0.003%, mainly second order.

德克斯 JCAD jcad.design The Netherlands		*Project* 0033/RO3	*Schematic* RO3_A
Title: MC stage (left)	Desc.: Transformer-less jfet based pre stage		
Designed by: JCA Dekkers	Rev.date: Feb 11, 2018	Revision: A	
Checked by:	PCB No:	Size: A3	
Approved by:	Sheet 8 of 10	1st.date: Nov 4, 2017	

Attenuator calculator: http://amorgignitamorem.nl/WebPaginas/Attenuator/AttenuatorAccordingToRonEnJacco.html



德克斯 JCAD jcad.design The Netherlands	Project 0033/RO3	Schematic RO3_A
Title: MC stage (right)	Desc.: Transformer-less jfet based pre stage	
Designed by: JCA Dekkers	Rev.date: Feb 11, 2018	Revision: A
Checked by:	PCB No:	Size: A3
Approved by:	Sheet 9 of 10	1st.date: Nov 4, 2017

德克斯	JCAD jcad.design The Netherlands	*Project* **0033/RO3**	*Schematic* RO3_A
Title: PS distribution	Desc.: Distribution of Local Power Supplies		
Designed by: JCA Dekkers	Rev.date: Feb 11, 2018	Revision: A	
Checked by:	PCB No:	Size: A3	
Approved by:	Sheet 10 of 10	1st.date: Nov 4, 2017	