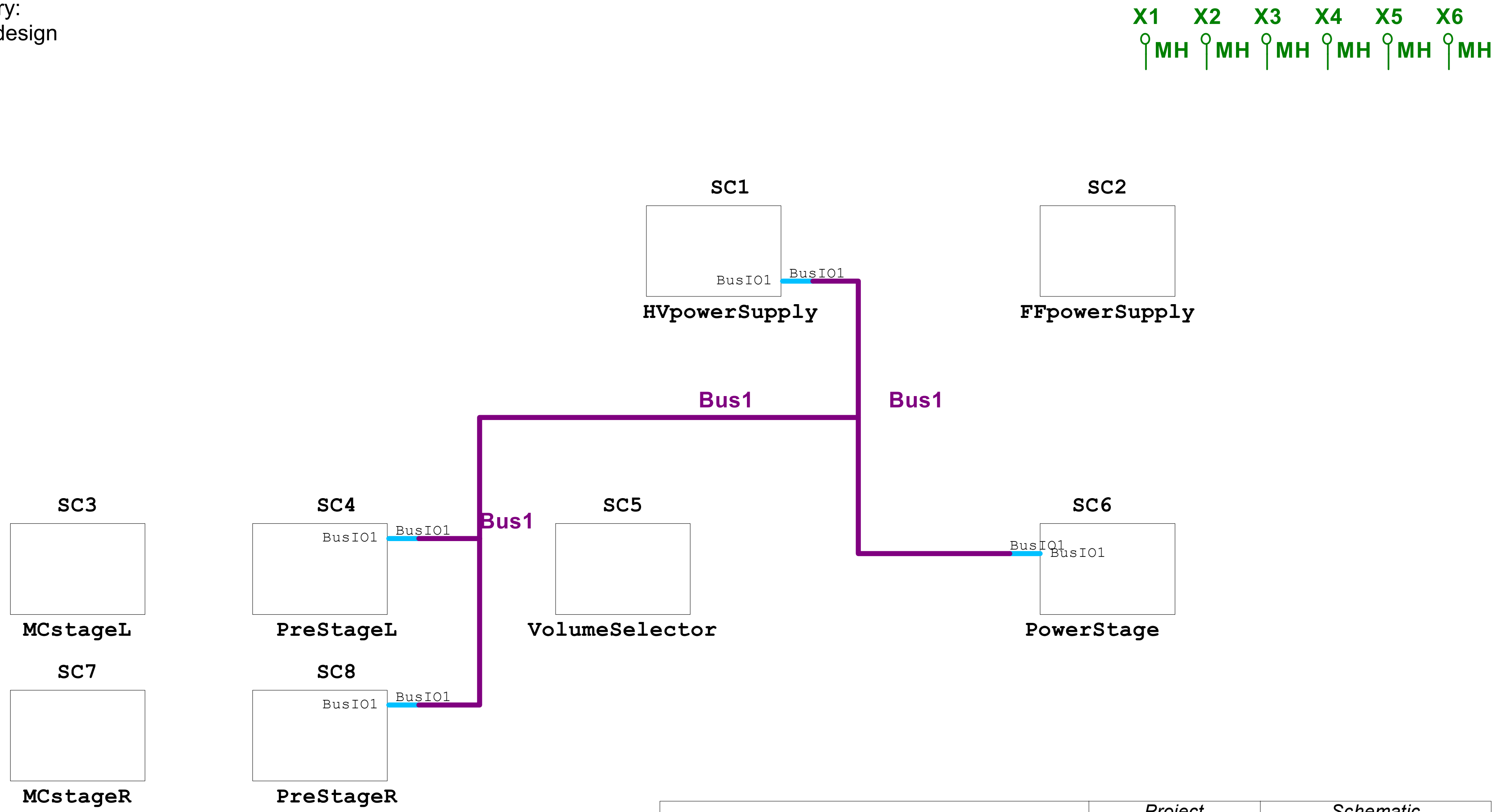
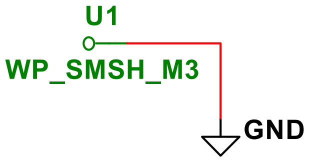
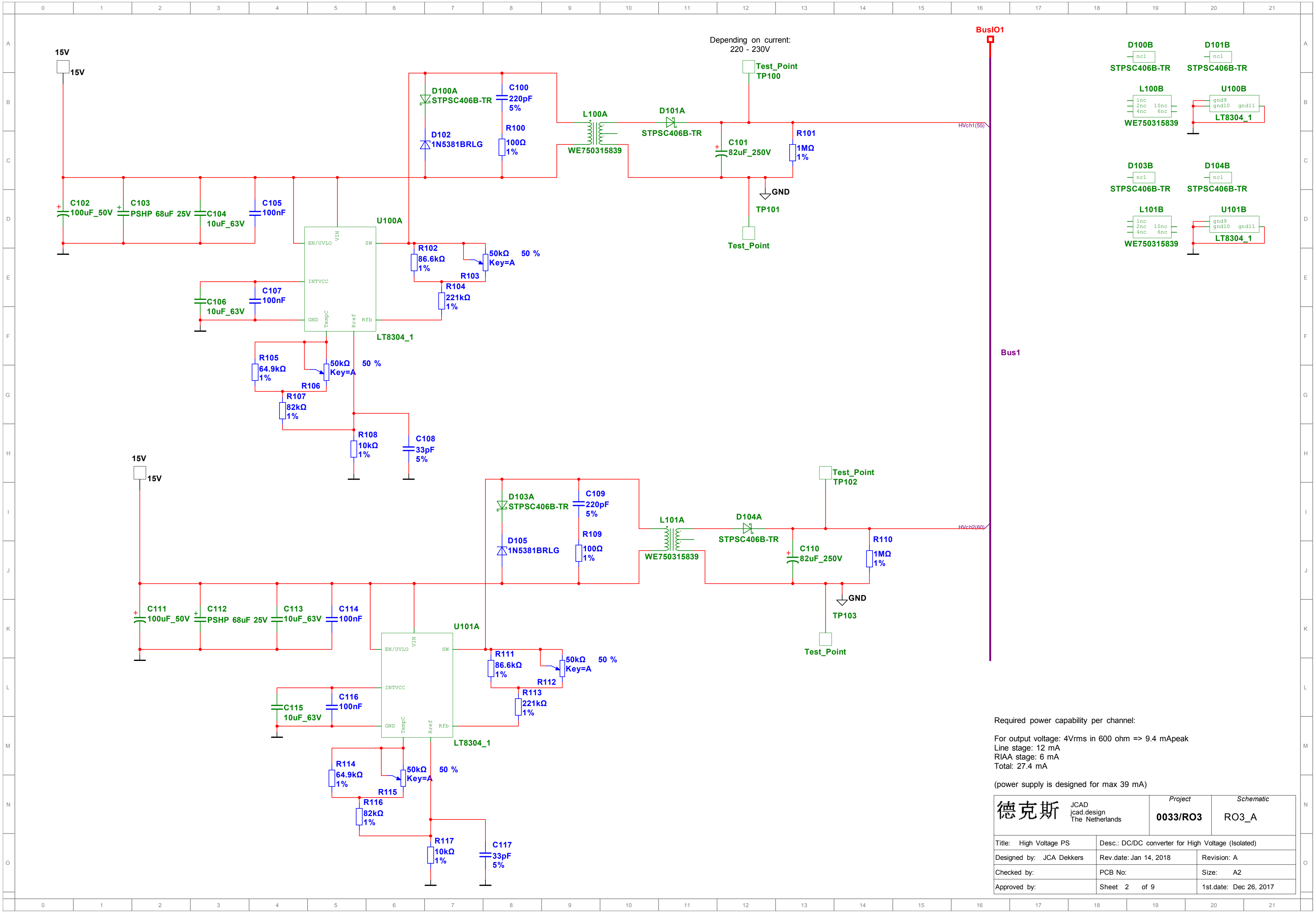
Revision History:
A Initial design





		Project	*Schematic*
德克斯	JCAD jcad.design The Netherlands	**0033/RO3**	RO3_A

Title: Functional Diagram	Desc.: Overview and Revision History	
Designed by: JCA Dekkers	Rev.date: Feb 04, 2018	Revision: A
Checked by:	PCB No:	Size: A4
Approved by:	Sheet 1 of 9	1st.date: Nov 4, 2017



Required power capability per channel:

For output voltage: 4Vrms in 600 ohm => 9.4 mApeak
Line stage: 12 mA
RIAA stage: 6 mA
Total: 27.4 mA

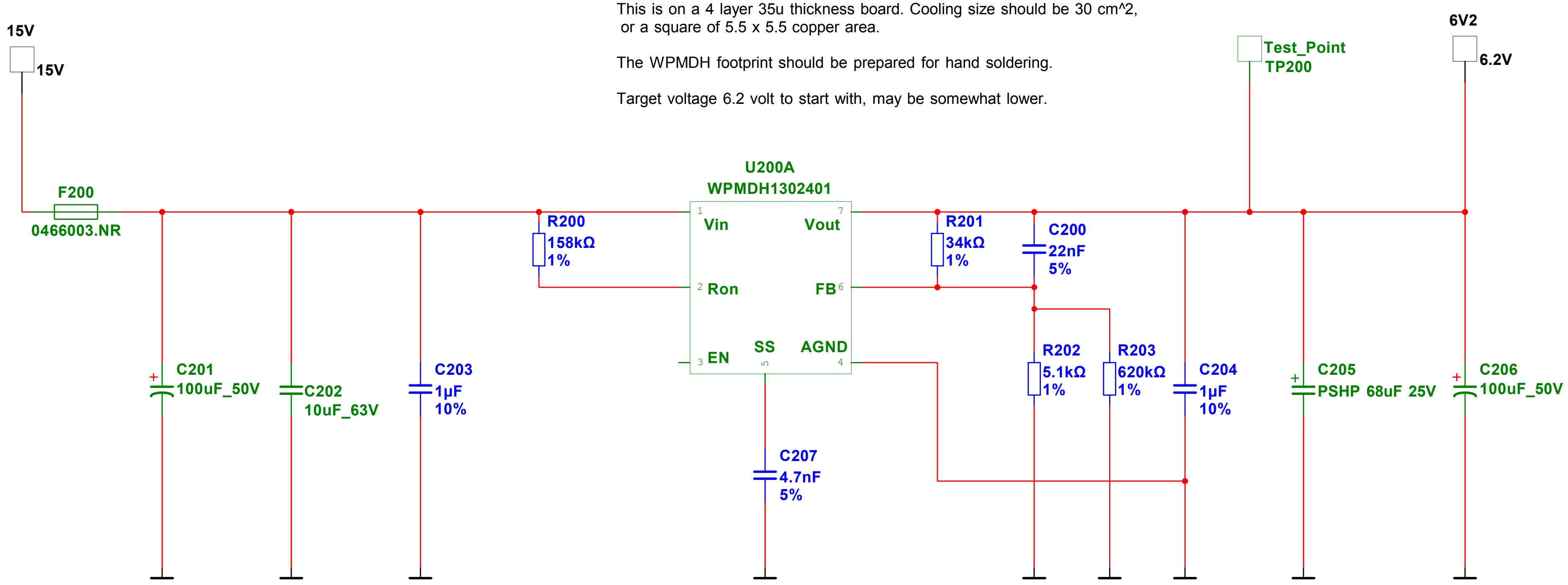
(power supply is designed for max 39 mA)

德克斯 JCAD jcad.design The Netherlands		Project 0033/RO3	Schematic RO3_A
Title: High Voltage PS	Desc.: DC/DC converter for High Voltage (Isolated)		
Designed by: JCA Dekkers	Rev.date: Jan 14, 2018		Revision: A
Checked by:	PCB No:		Size: A2
Approved by:	Sheet 2 of 9		1st.date: Dec 26, 2017

For 2.5 A ampere one needs 22 K/W thermal resisantce (see datasheet).
This is on a 4 layer 35u thickness board. Cooling size should be 30 cm^2,
or a square of 5.5 x 5.5 copper area.

The WPMDH footprint should be prepared for hand soldering.

Target voltage 6.2 volt to start with, may be somewhat lower.



AGND should be connected
to 1uF Cout as short as possible.

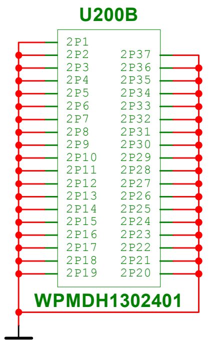
Design procedure:
1a. Rfbt/Rfbb = (Vout/0.803) - 1 = 6.72...
1b. Resistors should be between 1k ... 50k
1c. Choose Rfbt = 34k => Rfbb = 5.059 k

2a. Fsw(ccm) should be between 200kHz...800kHz, target 300kHz
2b. Ron = Vout/(1.3e-10 * Fsw(ccm)) => 158k
2c. Check whether Ron equal or greater than Vinmax*150e-9/1.3e-10 => okay!

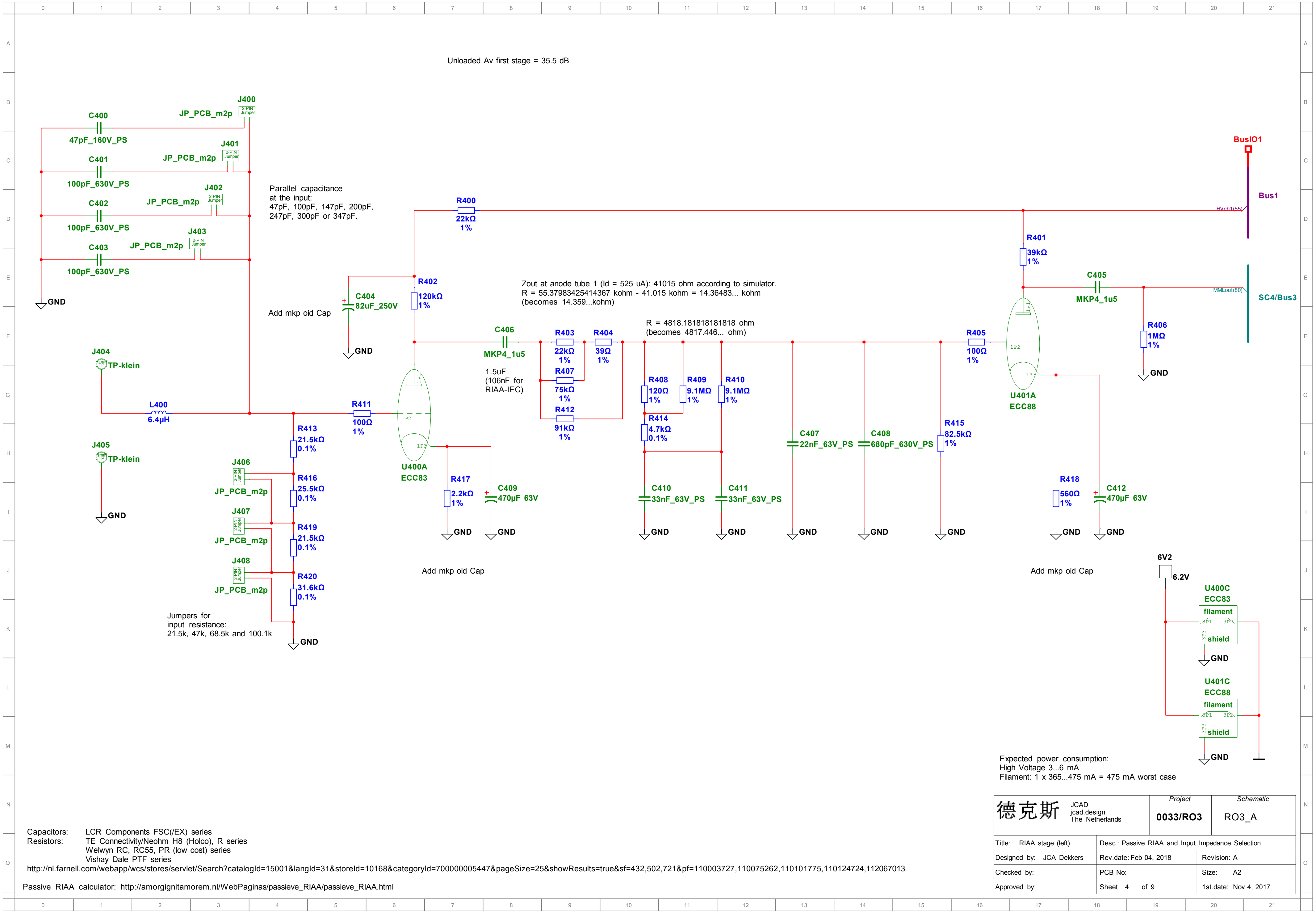
With Vin = 15, Vout = 6.2 and Fsw = 300k the DCM/CCM boundary is at approx 600 mA.

3a. Worst case input ripple current 0.5*Iout*sqrt(D/(1-D)) => 1.18 A. Input C should be able to withstand this.
3b. Value of Cin is related to the maximum DeltaVin: Cin equal or greater than Iout*D*(1-D)/(Fsw(ccm)*DeltaVin) => 100uF safe choice

Required power capability:
Filament: 6.3V at 2 x 1.095...1425 mA = 2.19...2.85 A

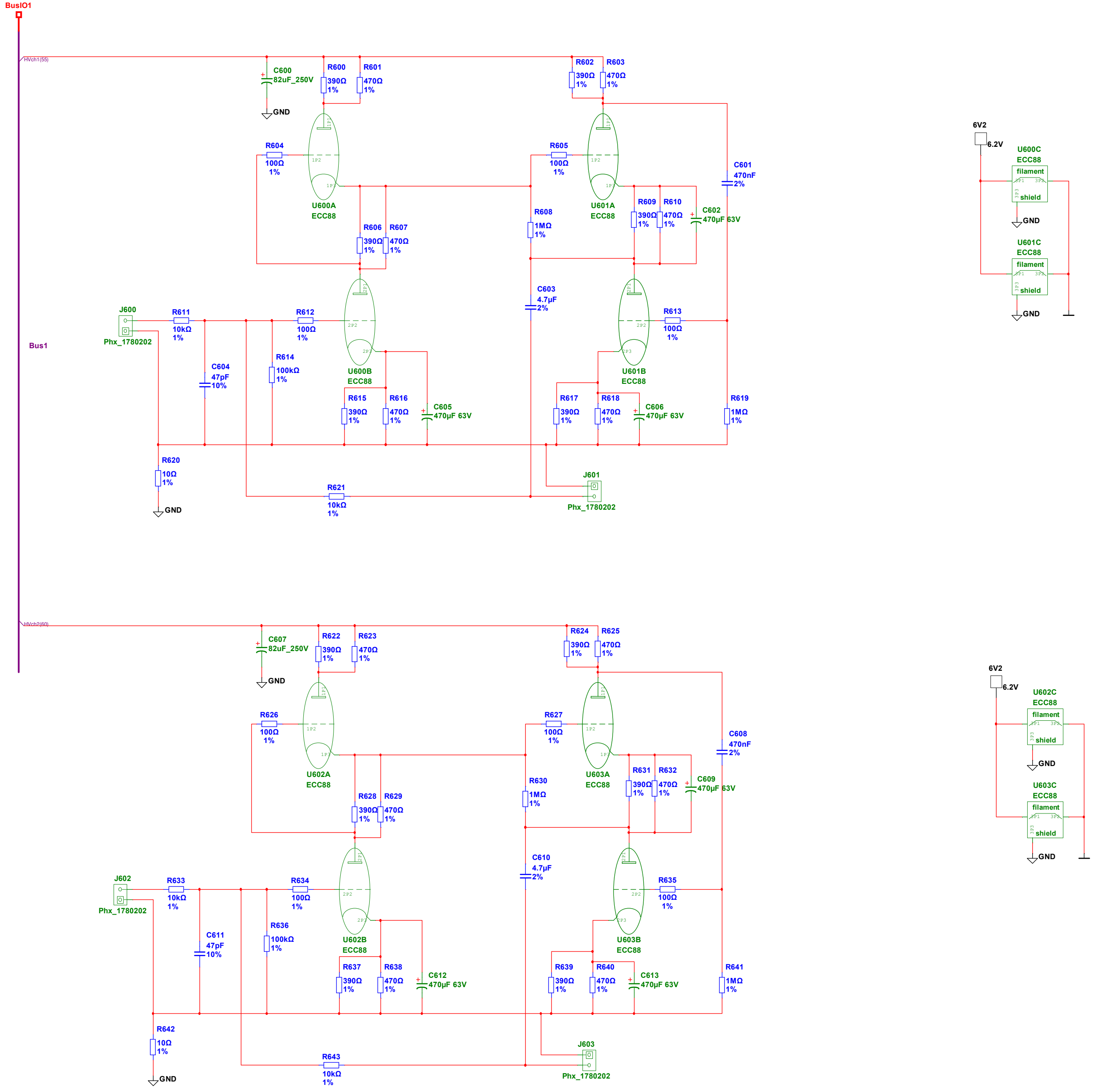


德克斯 JCAD jcad.design The Netherlands		*Project* 0033/RO3	*Schematic* RO3_A
Title: Filament PS	Desc.: DC/DC power supply for filaments		
Designed by: JCA Dekkers	Rev.date: Jan 14, 2018	Revision: A	
Checked by:	PCB No:	Size: A3	
Approved by:	Sheet 3 of 9	1st.date: Dec 24, 2017	



Unloaded Av first stage = 35.5 dB
C400
47pF_160V_PS
J400
JP_PCB_m2p
C401
100pF_630V_PS
J401
JP_PCB_m2p
C402
100pF_630V_PS
J402
JP_PCB_m2p
C403
100pF_630V_PS
J403
JP_PCB_m2p
GND
Parallel capacitance
at the input:
47pF, 100pF, 147pF, 200pF,
247pF, 300pF or 347pF.
R400
22kΩ
1%
BusIO1
Bus1
HVch1(55)
R401
39kΩ
1%
C405
MKP4_1u5
MMLout(80)
SC4/Bus3
R406
1MΩ
1%
Zout at anode tube 1 (Id = 525 uA): 41015 ohm according to simulator.
R = 55.37983425414367 kohm - 41.015 kohm = 14.36483... kohm
(becomes 14.359...kohm)
R = 4818.181818181818 ohm
(becomes 4817.446... ohm)
R402
120kΩ
1%
C404
82uF_250V
Add mkp oid Cap
C406
MKP4_1u5
1.5uF
(106nF for
RIAA-IEC)
R403
22kΩ
1%
R404
39Ω
1%
R407
75kΩ
1%
R412
91kΩ
1%
R405
100Ω
1%
J404
TP-klein
L400
6.4µH
J405
TP-klein
R411
100Ω
1%
U400A
ECC83
R417
2.2kΩ
1%
C409
470µF 63V
R408
120Ω
1%
R409
9.1MΩ
1%
R410
9.1MΩ
1%
R414
4.7kΩ
0.1%
C410
33nF_63V_PS
C411
33nF_63V_PS
C407
22nF_63V_PS
C408
680pF_630V_PS
R415
82.5kΩ
1%
U401A
ECC88
R418
560Ω
1%
C412
470µF 63V
R413
21.5kΩ
0.1%
J406
JP_PCB_m2p
R416
25.5kΩ
0.1%
J407
JP_PCB_m2p
R419
21.5kΩ
0.1%
J408
JP_PCB_m2p
R420
31.6kΩ
0.1%
Jumpers for
input resistance:
21.5k, 47k, 68.5k and 100.1k
Add mkp oid Cap
Add mkp oid Cap
6V2
6.2V
U400C
ECC83
filament
shield
U401C
ECC88
filament
shield
Expected power consumption:
High Voltage 3...6 mA
Filament: 1 x 365...475 mA = 475 mA worst case
Capacitors: LCR Components FSC(/EX) series
Resistors: TE Connectivity/Neohm H8 (Holco), R series
Welwyn RC, RC55, PR (low cost) series
Vishay Dale PTF series
http://nl.farnell.com/webapp/wcs/stores/servlet/Search?catalogId=15001&langId=31&storeId=10168&categoryId=700000005447&pageSize=25&showResults=true&sf=432,502,721&pf=110003727,110075262,110101775,110124724,112067013
Passive RIAA calculator: http://amorgignitamorem.nl/WebPaginas/passieve_RIAA/passieve_RIAA.html
德克斯
JCAD
jcad.design
The Netherlands
Project
0033/RO3
Schematic
RO3_A
Title: RIAA stage (left)
Desc.: Passive RIAA and Input Impedance Selection
Designed by: JCA Dekkers
Rev.date: Feb 04, 2018
Revision: A
Checked by:
PCB No:
Size: A2
Approved by:
Sheet 4 of 9
1st.date: Nov 4, 2017

德克斯 JCAD jcad.design The Netherlands		*Project* **0033/RO3**	*Schematic* RO3_A
Title: Input Selection	Desc.: RO3_A		
Designed by: JCA Dekkers	Rev.date: Jan 14, 2018	Revision: A	
Checked by:	PCB No:	Size: A3	
Approved by:	Sheet 5 of 9	1st.date: Nov 4, 2017	



Bandwidth 7 MHz

f = 1 kHz, B = 20 Hz - 30 kHz:

Vin,rms	Vout,rms	THD+N [%]	SNR [dB]
0.0707	0.0645	0.008	82.0
0.707	0.645	0.0023	98.6
2.0	1.82	0.0021	105.1
4.0	3.64	0.0038	101.2

With 50 ohm source and 2.2 kohm load (optimum load).

Vin,dc = 0 mV
Vout,dc = 0 mV

f = 1kHz at -0.92 dB, 20 Hz at -0.96 dB, 20 kHz at -0.92 dB, 100 kHz at -0.94 dB
Without feedback (R23 desoldered): Av = 25.56 dB at 1 kHz.

Rin = 10k4 (1 kHz), Rout = 36 ohm (20 Hz), 12 ohm (1 kHz and 10 kHz).

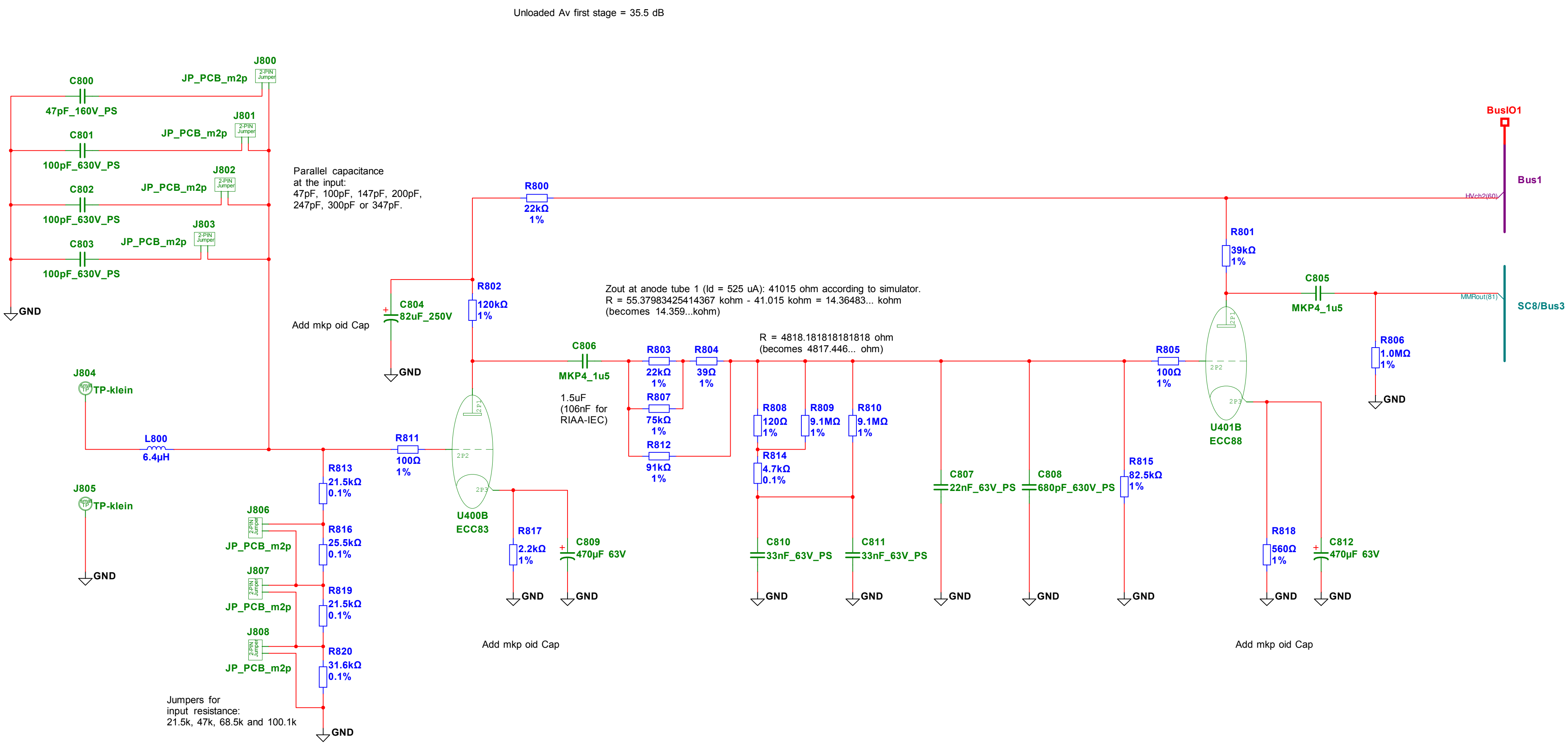
4u7:
Audyn Cap Plus, 1341762
D = 36mm, L = 63mm, d2 = 1.5mm

Audyn Cap Plus, 1341758
D = 25mm, L = 43mm, d2 = 1mm

Audyn Cap Plus, 1341755
D = 25mm, L = 43mm, d2 = 1mm

Expected power consumption:
High Voltage 12 mA
Filament: 2 x 365...475 mA = 950 mA worst case

德克斯 JCAD jcad.design The Netherlands	Project: 0033/RO3	Schematic: RO3_A
Title: Line Driver	Desc.: RO3_A	
Designed by: JCA Dekkers	Rev.date: Jan 14, 2018	Revision: A
Checked by:	PCB No:	Size: A1
Approved by:	Sheet 6 of 9	1st.date: Nov 4, 2017



Expected power consumption:
High Voltage 3...6 mA
Filament: 1 x 365...475 mA = 475 mA worst case

Capacitors: LCR Components FSC(/EX) series
Resistors: TE Connectivity/Neohm H8 (Holco), R series
Welwyn RC, RC55, PR (low cost) series
Vishay Dale PTF series
http://nl.farnell.com/webapp/wcs/stores/servlet/Search?catalogId=15001&langId=31&storeId=10168&categoryId=700000005447&pageSize=25&showResults=true&sf=432,502,721&pf=110003727,110075262,110101775,110124724,112067013

Passive RIAA calculator: http://amorgignitamorem.nl/WebPaginas/passieve_RIAA/passieve_RIAA.html

德克斯 JCAD jcad.design The Netherlands		Project 0033/RO3	Schematic RO3_A
Title: RIAA stage (right)	Desc.: Passive RIAA and Input Impedance Selection		
Designed by: JCA Dekkers	Rev.date: Feb 04, 2018	Revision: A	
Checked by:	PCB No:	Size: A2	
Approved by:	Sheet 7 of 9	1st.date: Nov 4, 2017	

A B C D E F

德克斯 JCAD jcad.design The Netherlands		*Project* **0033/RO3**	*Schematic* RO3_A
Title: MC stage (left)	Desc.: RO3_A		
Designed by: JCA Dekkers	Rev.date: Feb 04, 2018	Revision: A	
Checked by:	PCB No:	Size: A2	
Approved by:	Sheet 8 of 9	1st.date: Nov 4, 2017	

德克斯 JCAD jcad.design The Netherlands		*Project* **0033/RO3**	*Schematic* RO3_A
Title: MC stage (right)	Desc.: RO3_A		
Designed by: JCA Dekkers	Rev.date: Feb 04, 2018	Revision: A	
Checked by:	PCB No:	Size: A2	
Approved by:	Sheet 9 of 9	1st.date: Nov 4, 2017	